EGC220
Class Notes
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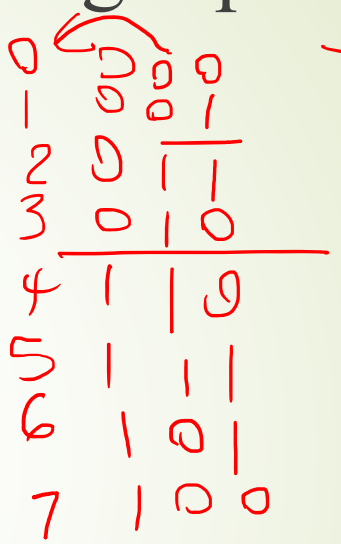
Test 2 will cover the following topics

- Design of combinational circuits
  - Circuit conversion to all NAND or NOR gates
- Design and use of
  - Multiplexers
  - Demultiplexers
  - Decoders
  - Encoders
- Design of combinational circuits using PLD's
- Latch and flip flops characteristics and timing.
- Design of ripple counters
- Analysis of sequential circuits



Closed book & Notes

Flip Flops Vs. Latches

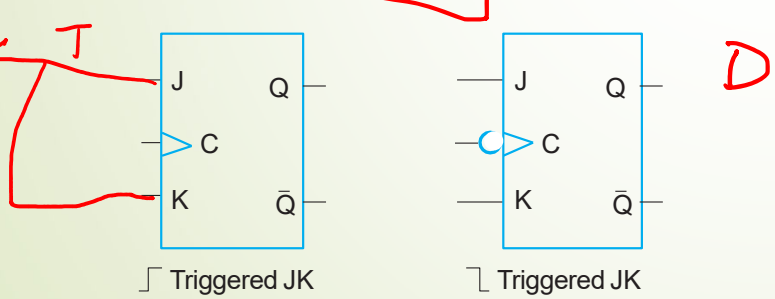
- Flip flops are Edge Triggered
- Latches are level triggered

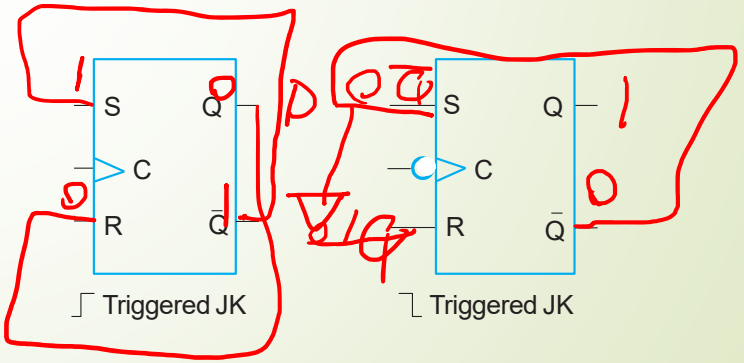
(a) *JK* Flip-Flop

J	K	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q}(t)$	Complement

(b) *SR* Flip-Flop

S	R	$Q(t+1)$	Operation
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

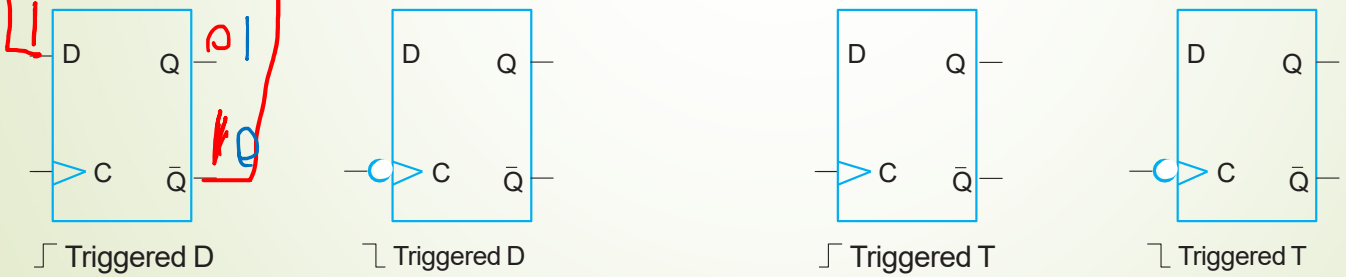




Flip Flops Vs. Latches

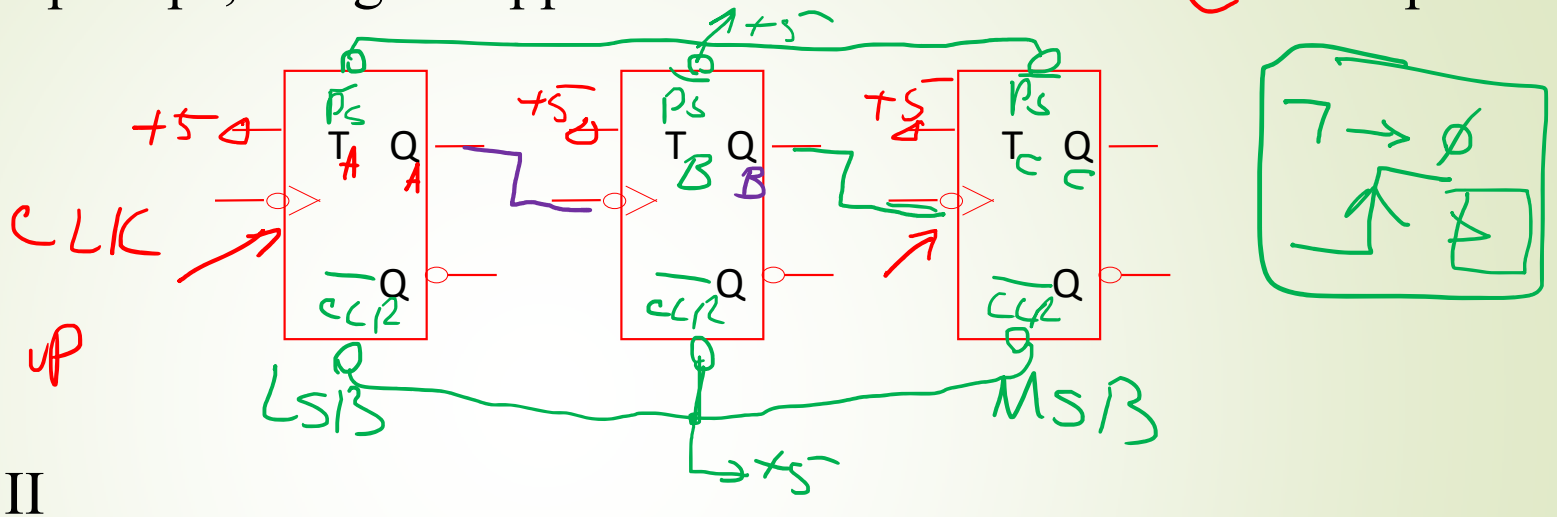
- Flip flops are Edge Triggered
- Latches are level triggered

(c) *D* Flip-Flop			(d) *T* Flip-Flop		
D	***Q* (*t* +1)**	**Operation**	**T**	***Q* (*t* +1)**	**Operation**
0	0	Reset	0	$Q(t)$	No change
1	1	Set	1	$\overline{Q(t)}$	Complement



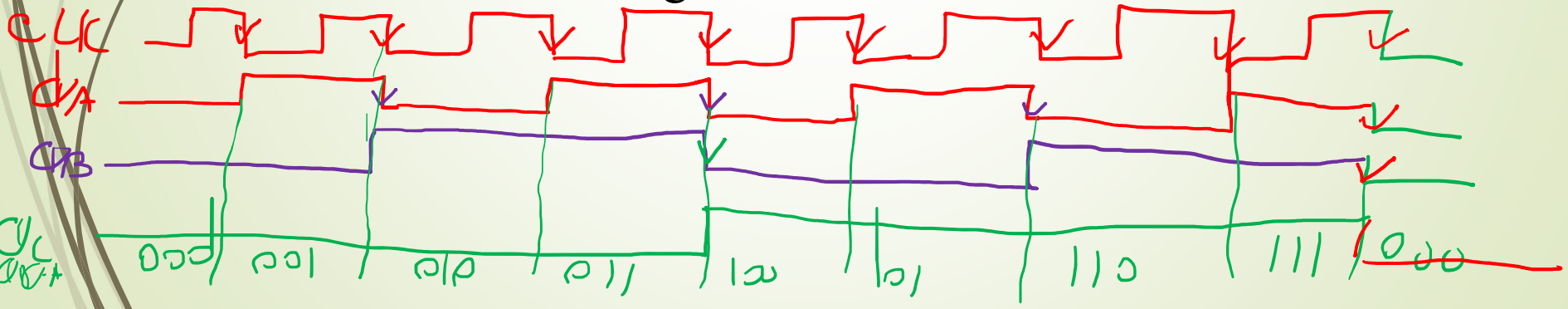
Problem I

Using T flip-flops, design a ripple counter that counts 0 – 7 and repeats.



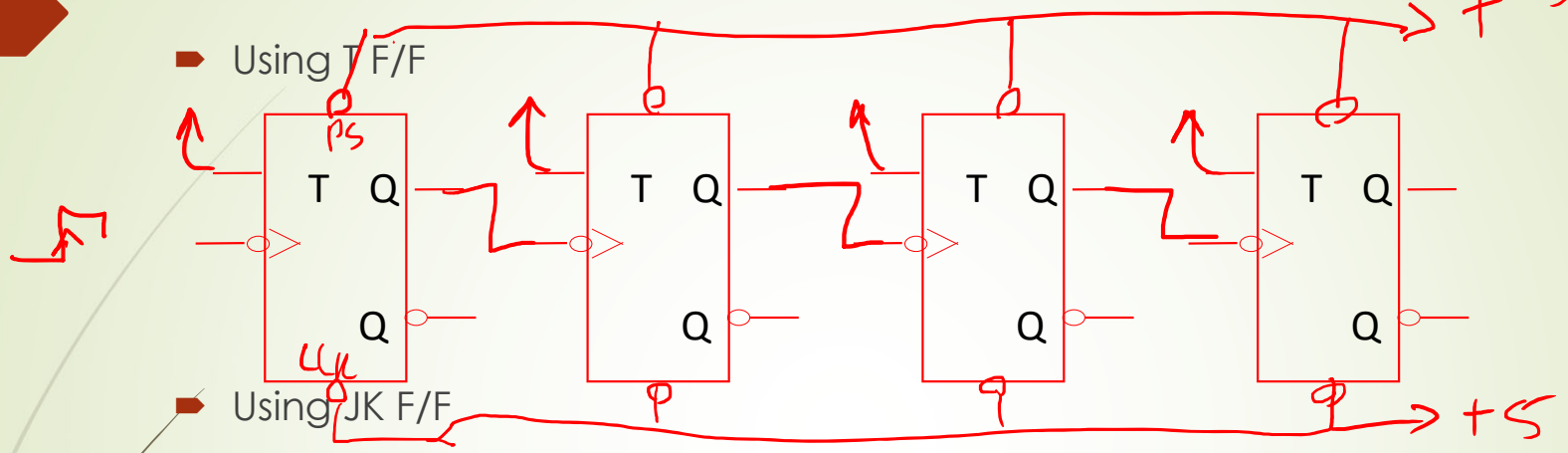
Problem II

Show the waveform diagram for the counter in Problem I.

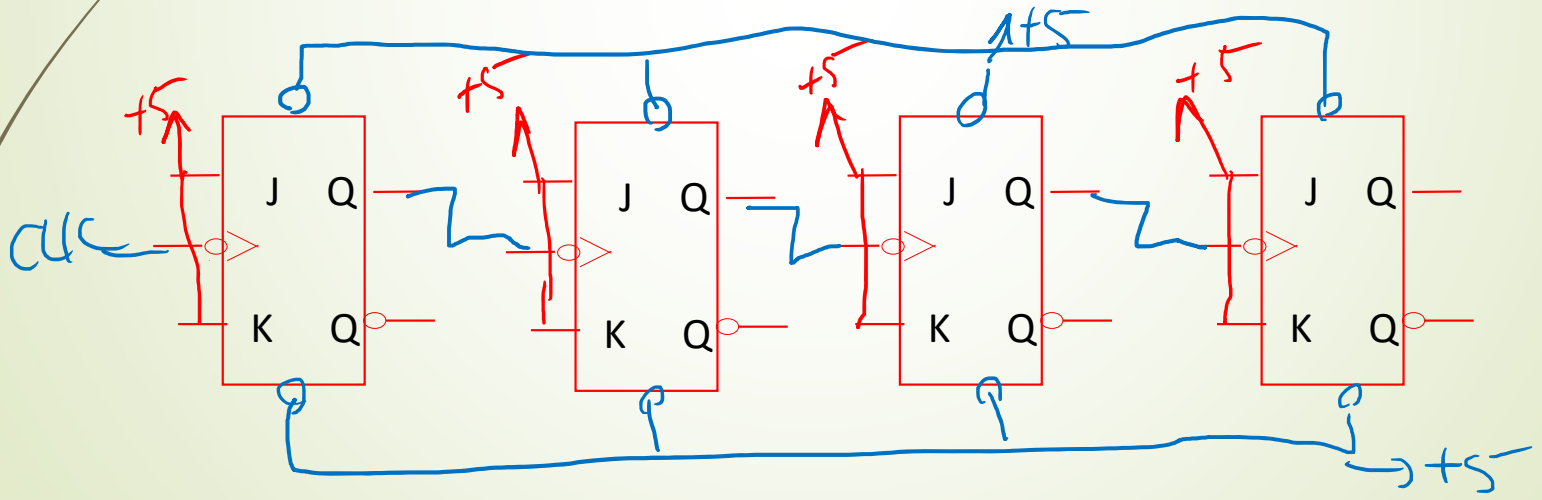


Design a Ripple Counter to count 0 to 15

- Using T F/F

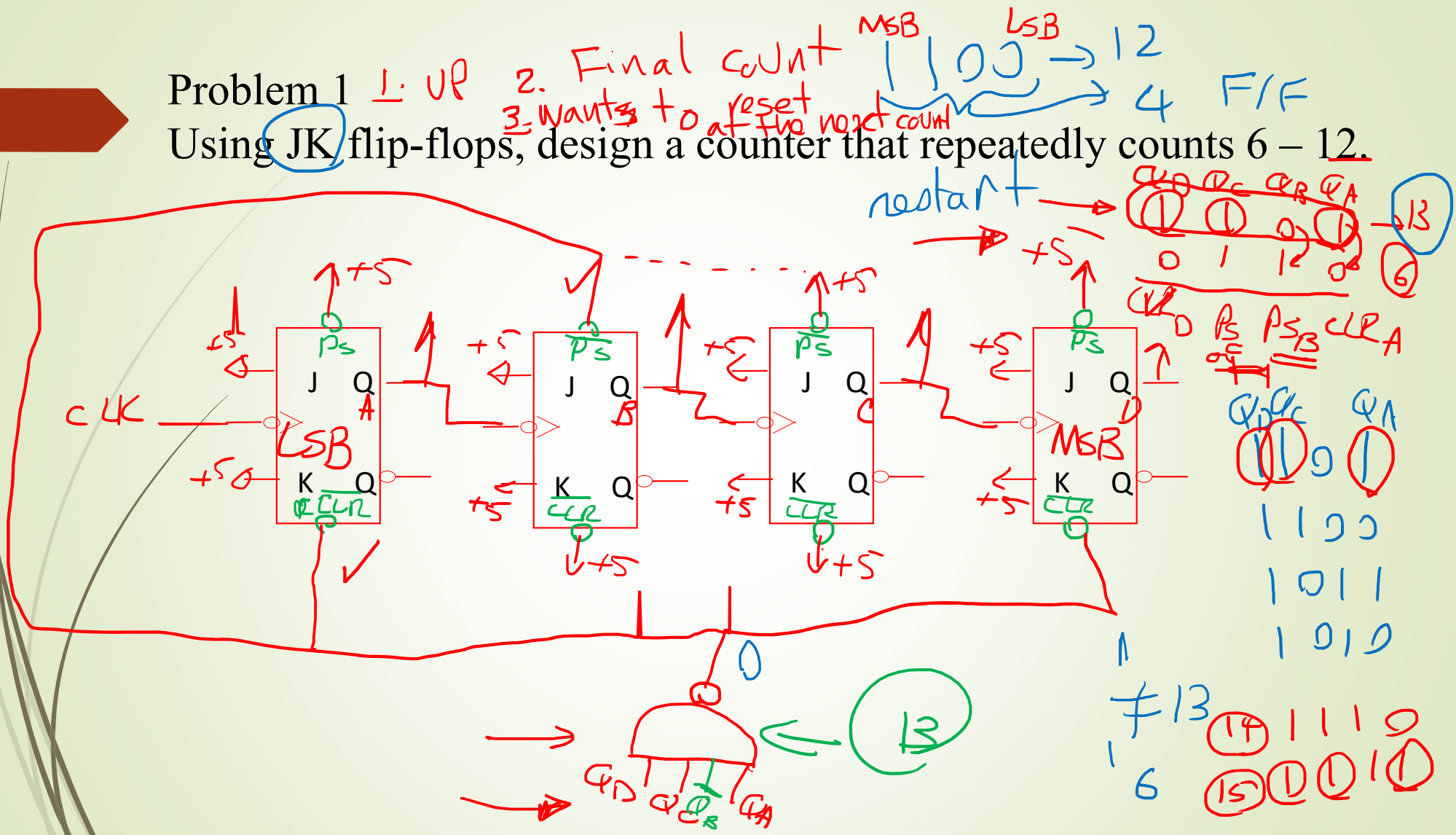


- Using JK F/F



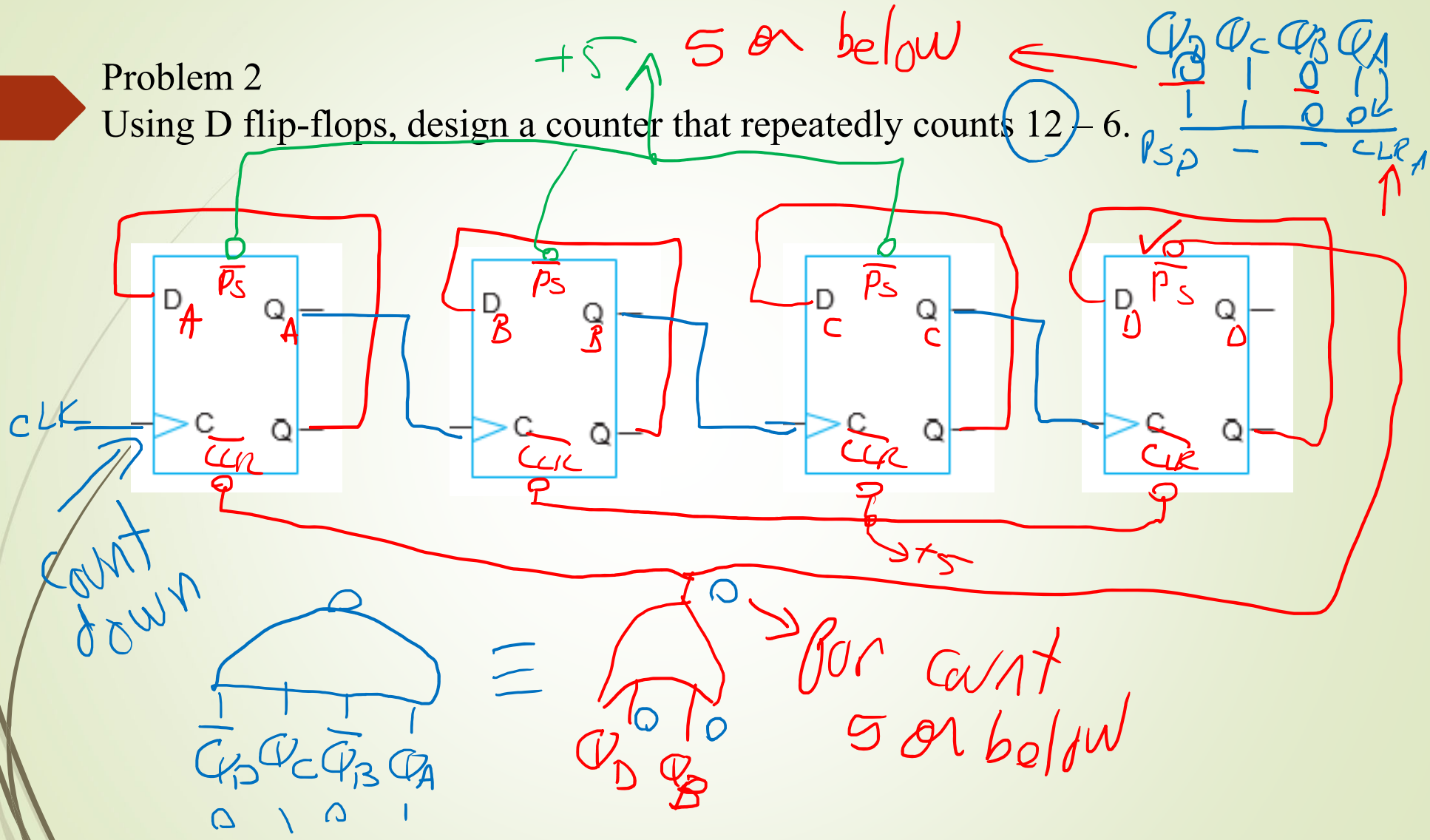
Problem 1

Using JK flip-flops, design a counter that repeatedly counts 6 – 12.



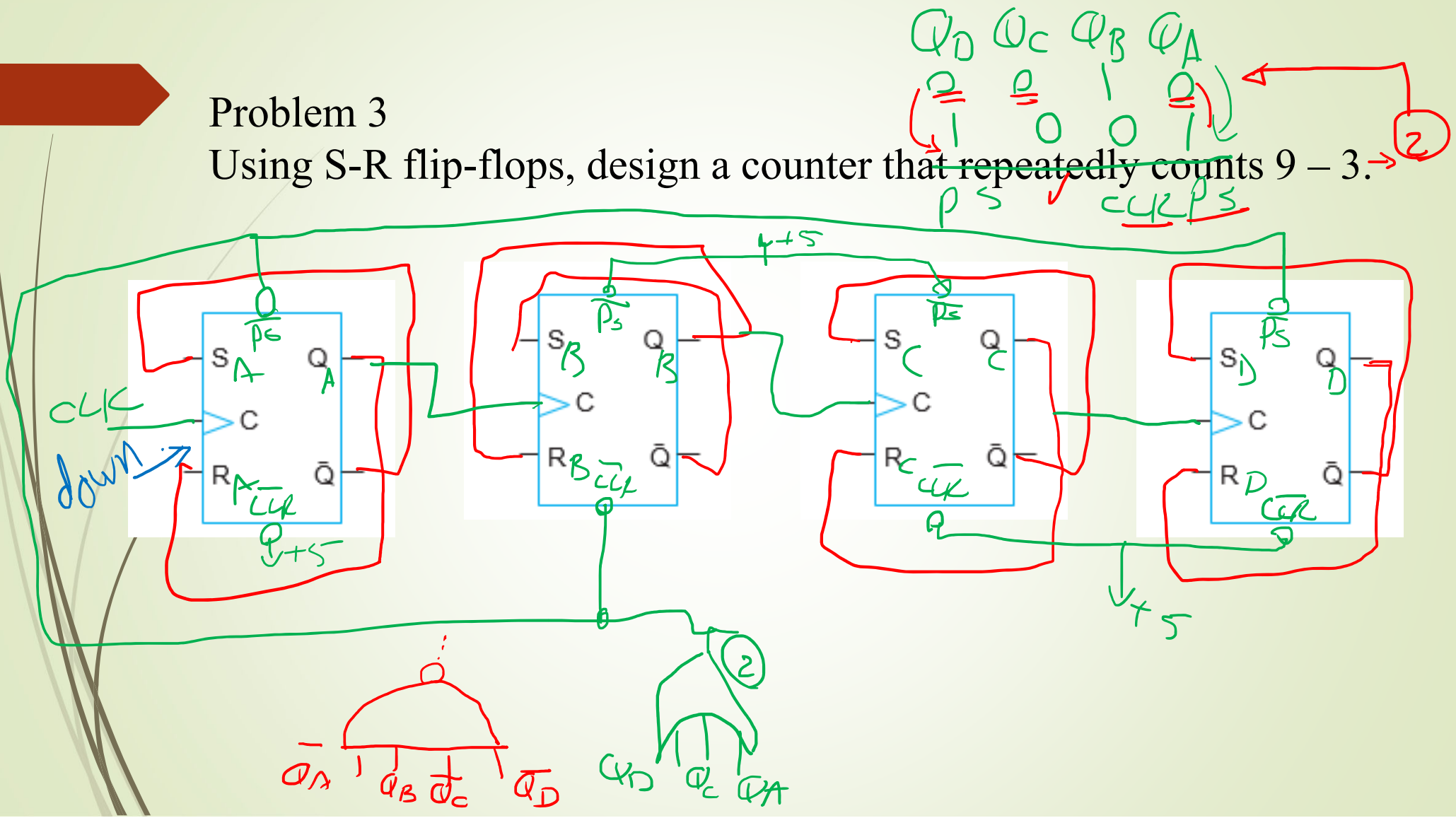
Problem 2

Using D flip-flops, design a counter that repeatedly counts 12 – 6.



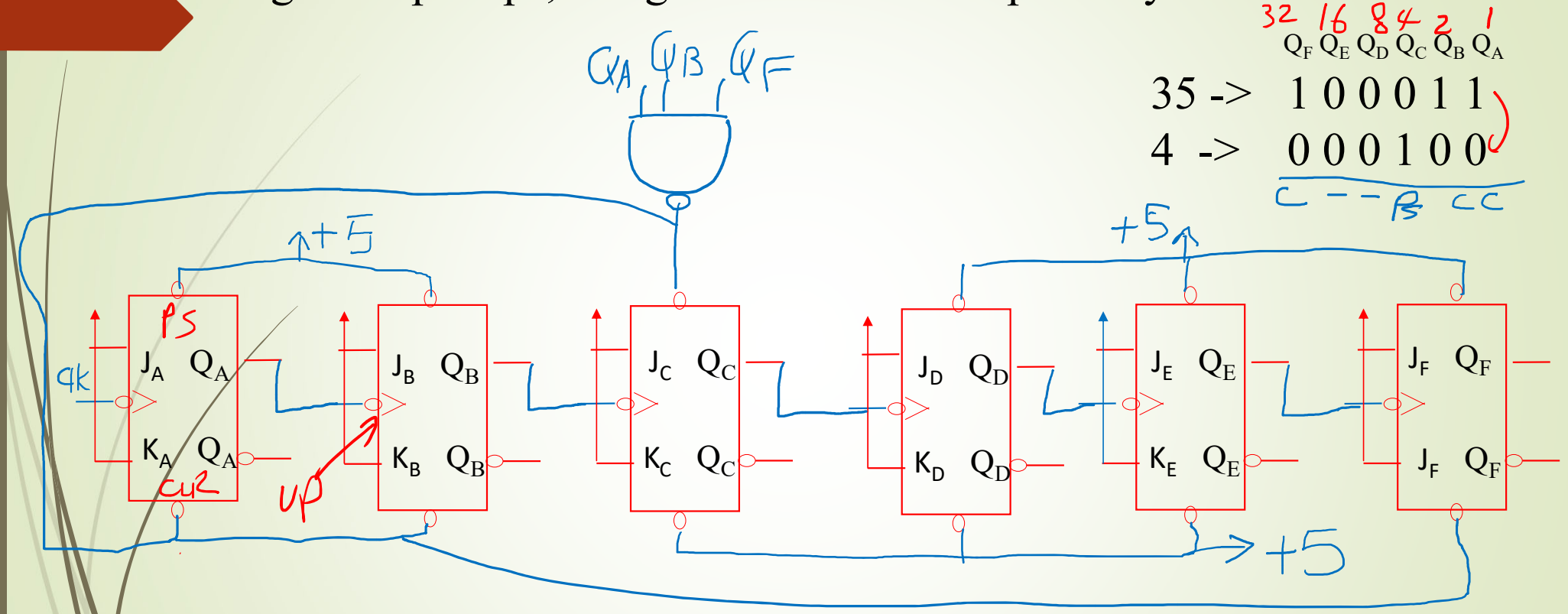
Problem 3

Using S-R flip-flops, design a counter that ~~repeatedly~~ counts 9 – 3.



Problem 4

Using JK flip-flops, design a counter that repeatedly counts 4 – 34



Problem 4

Using JK flip-flops, design a counter that repeatedly counts 34 – 4